P01	Bogdan J. Falkowski, Cicilia C. Lozano, Tadeusz Łuba	New Fastest Linearly Independent Transforms over GF(3)	EFALKOWSKI@ntu.edu.sg
P03	Bogdan J. Falkowski and Shixing Yan	Properties and Fast Algorithms for TernaryWalsh Transform	EFALKOWSKI@ntu.edu.sg
P05	Dan A. Simovici	On the Axiomatization of Generalized Entropic Metrics	dsim@cs.umb.edu
P06	Bogdan J. Falkowski, Cicilia C. Lozano, Tadeusz Łuba	Efficient Algorithm for Calculation of Quaternary Fixed Polarity Arithmetic Expansions	EFALKOWSKI@ntu.edu.sg
P07	Janusz Brzozowski, Yuli Ye	Simulation of Gate Circuits with Feedback in Multi-Valued Algebras	y3ye@cs.toronto.edu
P08	B.A.Romov	Restriction-closed Hyperclones	Bromov@aol.com
P10	Tsutomu Sasao	An Application of 16-Valued Logic to Design of Reconfigurable Logic Arrays	sasao@cse.kyutech.ac.jp
P11	Shinobu Nagayama,Tsutomu Sasao	Representations of Elementary Functions Using Edge-Valued MDDs	s_naga@ce.hiroshima-cu.ac.jp
P13	Lirigis Vasilios, Elena Dubrova	Evaluation and Comparison of Threshold Logic Gates	lirigisb@hotmail.com
P14	Yoshinori YAMAMOTO	Power Indexes in Voting Systems and Multiple-Valued Logic	yamamo@mti.biglobe.ne.jp
P16	Arnon Avron, Anna Zamansky	Many-valued Non-deterministic Effective Semantics for First-order Logics of Formal Inconsistency	zamalan@netvision.net.il
P17	Milena Stanković, Suzana Stojković, Claudio Moraga	LINEARIZATION OF TERNARY DECISION DIAGRAMS BY USING THE POLYNOMIAL CHRESTENSON SPECTRUM	mstankovic@elfak.ni.ac.yu
P19	Rusins Freivalds, Lıva Garkaje	Boolean functions of low polynomial degree for quantum query complexity theory	rusinsf@latnet.lv
P20	Yale Fan	A Generalization of the Deutsch-Jozsa Algorithm to Multi-Valued Quantum Logic	yalefan@gmail.com
P23	Heng Zhang, Mingyi Zhang, Benjuan Yang	Model-Characterizing Formulas and Normal Forms in G¨odel Logics	h.zhang@hotmail.com
P24	Claudio Moraga, Milena Stanković, Suzana Stojković	Spectral Analysis of Special Properties of Ternary Functions	claudio.moraga@udo.edu
P25	L. Haddad, H. Machida, I.G. Rosenberg	Monoidal Intervals of Partial Clones	haddad-l@rmc.ca
P26	Witold Charatonik, Michal Wrona	2-SAT Problems in Some Multi-valued Logics Based on Lattices	Witold.Charatonik@ii.uni.wroc.pl

P27	Rolf Drechsler, André Sülflow	Modeling a Fully Scalable Reed-Solomon Encoder/Decoder over GF(pm) in SystemC	suelflow@informatik.uni-bremen.de
P28	P. Eklund, M.A. Gal´an	The Rough Powerset Monad	magalan@ctima.uma.es
P29	Yukihiro Iguchi, Tsutomu Sasao, Munehiro Matsuura	On Designs of Radix Converters Using Arithmetic Decompositions	YRL04730@nifty.com
P30	Arushi Raghuvanshi, Yale Fan, Michal Woyke, Arvind Kumar!, Marek Perkowski	Quantum Robots for Teenagers	mperkows@ee.pdx.edu
P32	Naofumi Homma, Katsuhiko Degawa, Takafumi Aoki, Tatsuo Higuchi	Algorithm-level optimization of multiple-valued arithmetic circuits using counter tree diagrams	homma@aoki.ecei.tohoku.ac.jp
P34	Juan Núñez, José M. Quintana, María J. Avedillo	Limits to a Correct Evaluation in RTD-based Quaternary Inverters	jnunez@imse.cnm.es
P35	Radomir S. Stankovi´c, Jaakko Astola	Reading the Sampling Theorem in Multiple-Valued Logic	rstankovic@bankerinter.net
P36	Radomir S. Stankovi´c, Jaakko Astola	A Note on Possible Applications of Fourier Representations in Circuit Design over Reprogrammable Technological Platforms	rstankovic@bankerinter.net
P38	Krzysztof S. Berezowski, Sarma B. K. Vrudhula	Multiple-Valued Logic Circuits Design using Negative Differential Resistance Devices	krzysztof.berezowski@pwr.wroc.pl
P39	Ricardo Cunha G. da Silva, Henri Boudinov	Quaternary Look-up Tables using voltage-mode CMOS Logic Design	ricardo@if.ufrgs.br
P40	Viorica Sofronie-Stokkermans, Carsten Ihlemann	Automated reasoning in some local extensions of ordered structures	sofronie@mpi-sb.mpg.de
P41	Tomohiro Takahashi, Kazuyasu Mizusawa, Takahiro Hanyu	Asynchronous Peer-to-Peer Simplex/Duplex-Compatible Communication System Using a One-Phase Signaling Scheme	takahasi@ngc.riec.tohoku.ac.jp
P42	Lucien Haddad, Dietlinde Lau	Characterization of Partial She®er Functions in 3-valued Logic	haddad-l@rmc.ca
P43	Dragan Janković, Radomir S. Stanković, Claudio Moraga	Exploiting of Homogeneous Dual Polarity Routes in Implementation of Algorithms for Optimization of Galois Field Expressions for Ternary Functions	rstankovic@bankerinter.net

P45	D. Michael Miller, David Y. Feinstein, Mitchell A. Thornton	Variable Reordering and Sifting for QMDD	mmiller@cs.uvic.ca
P48	Hirokatsu Shirahama, Akira Mochizuki, Takahiro Hanyu, Masami Nakajima, Kazutami Arimoto	Design of a Processing Element Based on Quaternary Differential Logic for a Multi-Core SIMD Processor	shira@ngc.riec.tohoku.ac.jp
P49	Akira Mochizuki, Masatomo Miura, Takahiro Hanyu	Active-Load Differential Comparator for Crosstalk-Noise Reduction	miura@ngc.riec.tohoku.ac.jp
P50	Yasushi YUMINAKA, Kazuyoshi YAMAMURA	Equalization Techniques for Multiple-Valued Data Transmission and Their Application	yuminaka@el.gunma-u.ac.jp
P51	Mozammel H. A. Khan, Marek A. Perkowski	GF(4) Based Synthesis Of Quaternary Reversible/Quantum Logic Circuits	mhakhan@ewubd.edu
P52	Igor Aizenberg, Claudio Moraga	The Genetic Code as a Multiple-Valued Function and its implementation Using Multilayer Neural Network based on Multi-Valued Neurons	Igor.Aizenberg@tamut.edu
P53	Mahsan Amoui, Daniel Große, Mitchell A. Thornton, Rolf Drechsler	Evaluation of Toggle Coverage for MVL Circuits Specified in the SystemVerilog HDL	mahsan@engr.smu.edu
P54	Motoi INABA	Experiment Result of Down Literal Circuit and Analog Inverter on CMOS Double-Polysilicon Process	inaba@a.tsukuba-tech.ac.jp
P55	Nobuaki Okada, Michitaka Kameyama	Low-Power Multiple-Valued Reconfigurable VLSI Using Series-Gating Differential-Pair Circuits	nokada@kameyama.ecei.tohoku.ac.jp
P56	Tetsuya Uemura, Takao Marukame, Ken-ichi Matsuda, Masafumi Yamamoto	Four-state Magnetic Random Access Memory and Ternary Content Addressable Memory using CoFe-based Magnetic Tunnel Junctions	uemura@ist.hokudai.ac.jp
P58	Yngvar Berg, Rene Jensen, Johannes Goplen Lomsdalen, Henning Gundersen, Snorre Aunet	Fault tolerant CMOS logic using ternary gates.	yngvarb@ifi.uio.no
P60	Stephan Eggersglüß, Daniel Tille, Görschwin Fey, Rolf Drechsler, Andreas Glowatz Friedrich Hapke Jürgen Schlöffel	Experimental Studies on SAT-based ATPG for Gate Delay Faults	segg@informatik.uni-bremen.de
P61	Tasuku Ito, Michitaka KameyamaTasuku Ito and Michitaka Kameyama	Universal VLSI Based on a Redundant Multiple-Valued Sequential Logic Operation	task@kameyama.ecei.tohoku.ac.jp

P62	Mostafa Abd-El-Barr, Bambang A. B. Sarif	Fuzzy Weighted and Ordered Direct Cover Algorithms for Minimization of MVL Functions	sarif@ccse.kfupm.edu.sa
P64	Dietlinde Lau, Masahiro Miyakawa	Classifications and basis enumerations in P3(2)	dietlinde.lau@uni-rostock.de
P65	Asif I. Khan, Nadia Nusrat, Samira M. Khan, Masud Hasan, Mozammel H. Khan	Quantum Realization of Some Ternary Circuits using Muthukrishnan-Stroud Gates	masudhasan@cse.buet.ac.bd
P66	Jun Liu, Luis Martinez, and Yang Xu	Automated Reasoning Algorithm for Linguistic Valued Łukasiewicz Propositional Logic	j.liu@ulster.ac.uk
P67	Saeed Sharifi Tehrani, Shie Mannor, Warren J. Gross	Survey of Stochastic Computation on Factor Graphs	saeed.sharifitehrani@mail.mcgill.ca
P68	Donglin Li, Otmane Ait-Mohamed, Sa'ed Abed	Towards First-Order Symbolic Trajectory Evaluation	s_abed@encs.concordia.ca
P69	Martin Lukac, Marek Perkowski	Quantum mechanical model of emotional robot behaviors	lukacm@cecs.pdx.edu
P70	Henning Gundersen, Yngvar Berg	Fast Addition Using Balanced Ternary Counters Designed with CMOS Semi-Floating Gate Devices	henningg@ifi.uio.no
P71	Tomoki Tanoue, Munehiko Nagatani, Takao Waho	A Ternary Analog-to-Digital Converter System	Twaho8@aol.com
P72	Hajime Machida, Michael Pinsker	Polynomials as Generators of Minimal Clones	machida@math.hit-u.ac.jp
P73	Carlos Ansótegui, Maria Luisa Bonet, Jordi Levy and Felip Manyà	A Complete Resolution Calculus for Signed Max-SAT	carlos@diei.udl.es
P74	Nabil Abu-Khader, Pepe Siy	Inversion/Division in Galois Field Using Multiple-Valued Logic	ah7267@wayne.edu
P75	René Jensen and Yngvar Berg	Configurable Multiple-Valued Encoders using Semi Floating-Gate Inverters	renej@student.matnat.uio.no