ISMVL-2007 Program at a glance

Day	*Morning*		*Afternoon*	
ULSIWS **May 13** *University of Oslo*	**ULSI Workshop (10:30 – 16:05)** ***(Informatics building, Lille Auditorium)***			
ISMVL **May 14** *Scandic Edderkoppen Hotel*	(08:00-08:45) **Registration** (08:45-08:50) **Opening Address** (08:50-10:00) **Keynote Address** (Valeriu B. Beiu) *Coffe break (10:00-10:05)*	(10:05-11:05) **Session 1A** **Theory 1** **Session 1B** **Logic Functions** *Coffe break (11:05-11:10)* (11:10-12:10) **Session 2A** **Theory 2- Clones** **Session 2B** **Quantum Computing 1** *Lunch (12:10-13:30)*	(13:30-14:50) **Session 3A** **Theory 3** **Session 3B** **Quantum Computing 2** *Coffe break (14:50-15:00)* (15:00-16:00) **Session 4A** **Theory 4** **Session 4B** **Circuit Design 1** *Cofee break (16:00:16:10)*	(16:10-17:10) **Session 5A** **Theory 5** **Session 5B** **Circuit Design 2** *(19:00-20.45)* *Guided tour in downtown Oslo* (21:00-22:00) *Reception at the Oslo City Hall*
ISMVL **May 15** *Scandic Edderkoppen Hotel*	**Invited Address** (08:45-10:00) (Mark Glusker) *Coffe break (10:00-10:05)*	(10:05-11:05) **Session 6A** **Theory 6** **Session 6B** **Circuit Design 3** *Coffe break (11:05-11:10)* (11:10-12:10) **Session 7A** **Theory 7** **Session 7B** **Circuit Design 4** *Lunch (12:10-13:30)*	(13:30-14:50) **Session 8A** **Theory 8** **Session 8B** **Circuit Design 5** *Coffe break (14:50-15:00)* (15:00-16:00) **Session 9A** **Circuit Design 6** **Session 9B** **Circuit Design 7** *Cofee break (16:00:16:10)*	(16:10-17:10) **Plenary Session** *(18:30-19:30)* *Guided bus tour in the surrondings of Oslo* *(19:30-24:00)* *Banquet at Frognerseteren Restaurant* **Closing**
RM2007 **May 16** *University of Oslo*	**Reed-Muller Workshop (09:00-17:15)** ***(Administration building, Rådssalen)***			
May 17	**The Norwegian Independence Day, 17th May** *If you stay for an extra day, you will get the possibility to experience the 17th of May Celebration.*			

ISMVL-2007 Program

May 14, Morning, Scandic Edderkoppen Hotel

08:00 - 08:45 Registration

08:45 - 08:50 Opening Address

08:50 - 10:00 Keynote Address

Grand Challenges of Nanoelectronics and Possible Architectural Solutions
Valeriu B. Beiu

10:00 - 10:05 Coffee Break

10:05 - 11:05 Session 1A and 1B

Session 1A – Theory *(Chair: D. Simovici)*
Automated reasoning in some local extensions of ordered structures
Viorica Sofronie-Stokkermans, Carsten Ihlemann

Reading the Sampling Theorem in Multiple-Valued Logic
Radomir S. Stankovi´c, Jaakko Astola

Model-Characterizing Formulas and Normal Forms in Gödel Logics
Heng Zhang, Mingyi Zhang, Benjuan Yang

Session 1B – Logic Functions*(Chair: B. Steinbach)*
Spectral Analysis of Special Properties of Ternary Functions
Claudio Moraga, Milena Stanković, Suzana Stojković

Representations of Elementary Functions Using Edge-Valued MDDs
Shinobu Nagayama,Tsutomu Sasao

Experimental Studies on SAT-based ATPG for Gate Delay Faults
Stephan Eggersglüß, Daniel Tille, Görschwin Fey, Rolf Drechsler, Andreas Glowatz, Friedrich Hapke, Jürgen Schlöffel

11:05 - 11:10 Coffee Break

11:10 - 12:10 Session 2A and 2B

Session 2A – Theory 2 – Clones *(Chair: M. Miyakawa)*
Polynomials as Generators of Minimal Clones
Hajime Machida, Michael Pinsker

Restriction-closed Hyperclones
B.A.Romov

Monoidal Intervals of Partial Clones
L. Haddad, H. Machida, I.G. Rosenberg

Session 2B – Quantum Computing 1 *(Chair: B. Falkowski)*
Variable Reordering and Sifting for QMDD
D. Michael Miller, David Y. Feinstein, Mitchell A. Thornton

GF(4) Based Synthesis Of Quaternary Reversible/Quantum Logic Circuits
Mozammel H. A. Khan, Marek A. Perkowski

A Generalization of the Deutsch-Jozsa Algorithm to Multi-Valued Quantum Logic
Yale Fan

12:10 – 13:30 Lunch (at Scandic Edderkoppen Hotel)

May 14, Afternoon, Scandic Edderkoppen Hotel

13:30 – 14:50 Session 3A and 3B

Session 3A – Theory 3*(Chair: C. Ihlemann)*
The Genetic Code as a Multiple-Valued Function and its implementation Using Multilayer Neural Network based on Multi-Valued Neurons
Igor Aizenberg, Claudio Moraga

Many-valued Non-deterministic Effective Semantics for First-order Logics of Formal Inconsistency
Arnon Avron, Anna Zamansky

New Fastest Linearly Independent Transforms over GF(3)
Bogdan J. Falkowski, Cicilia C. Lozano, Tadeusz Łuba

Inversion/Division in Galois Field Using Multiple-Valued Logic
Nabil Abu-Khader, Pepe Siy

Session 3B - Quantum Computing 2 *(Chair: M. Miller)*
Boolean functions of low polynomial degree for quantum query complexity theory
Rusins Freivalds, Lıva Garkaje

Quantum Robots for Teenagers
Arushi Raghuvanshi, Yale Fan, Michal Woyke, Marek Perkowski

Quantum mechanical model of emotional robot behaviors
Martin Lukac, Marek Perkowski

Quantum Realization of Some Ternary Circuits using Muthukrishnan-Stroud Gates
Asif I. Khan, Nadia Nusrat, Samira M. Khan, Mozammel H. Khan

14:50 - 15:00 Coffee Break

15:00 – 16:00 Session 4A and 4B

Session 4A – Theory 4 *(Chair: A. Zamansky)*
2-SAT Problems in Some Multi-valued Logics Based on Lattices
Witold Charatonik, Michal Wrona

A Complete Resolution Calculus for Signed Max-SAT
Carlos Ansótegui, Maria Luisa Bonet, Jordi Levy and Felip Manyà

Efficient Algorithm for Calculation of Quaternary Fixed Polarity Arithmetic Expansions
Bogdan J. Falkowski, Cicilia C. Lozano, Tadeusz Łuba

Session 4B – Circuit Design 1 *(Chair: T. Sasao)*
Multiple-Valued Logic Circuits Design using Negative Differential Resistance Devices
Krzysztof S. Berezowski, Sarma B. K. Vrudhula

Low-Power Multiple-Valued Reconfigurable VLSI Using Series-Gating Differential-Pair Circuits
Nobuaki Okada, Michitaka Kameyama

Equalization Techniques for Multiple-Valued Data Transmission and Their Application
Yasushi Yuminaka, Kazuyoshi Yamamura

16:00 - 16:10 Coffee Break

16:10 – 17:10 Session 5A and 5B

Session 5A – Theory 5 *(Chair: M. Wrona)*
The Rough Powerset Monad
P. Eklund, M.A. Galàn

Exploiting of Homogeneous Dual Polarity Routes in Implementation of Algorithms for Optimization of Galois Field Expressions for Ternary Functions
Dragan Janković, Radomir S. Stanković, Claudio Moraga

Automated Reasoning Algorithm for Linguistic Valued Łukasiewicz Propositional Logic
Jun Liu, Luis Martinez, and Yang Xu

Session 5B – Circuit Design 2 *(Chair: Y. Yuminaka)*
Fast Addition Using Balanced Ternary Counters Designed With CMOS Semi-Floating Gate Devices
Henning Gundersen, Yngvar Berg

Algorithm-level optimization of multiple-valued arithmetic circuits using counter tree diagrams
Naofumi Homma, Katsuhiko Degawa, Takafumi Aoki, Tatsuo Higuchi

On Designs of Radix Converters Using Arithmetic Decompositions
Yukihiro Iguchi, Tsutomu Sasao, Munehiro Matsuura

19:00 – 20:45 A guided tour in downtown Oslo.

We take a nice walk through the streets of Oslo. Starting from the Scandic Edderkoppen Hotel and ending up at the Oslo City Hall. We look at the attractions situated at the heart of the city, The Royal Castle, Karl Johan Street, Akershus Fortress, and Aker Brygge.

21:00 – 22:00 Reception at the Oslo City Hall

The city of Oslo invites all participants at the conference to a reception at the Oslo City Hall. The mayor of Oslo will personally welcome guests to the exquisite City Hall. Snacks and beverages will be served.

May 15, Morning, Scandic Edderkoppen Hotel

08:45 - 10:00 Invited Address

The Ternary Calculating Machine of Thomas Fowler
M. Glusker

10:00 - 10:05 Coffee Break

10:05 - 11:05 Session 6A and 6B

Session 6A – Theory 6 *(Chair: H. Machida)*
On the Axiomatization of Generalized Entropic Metrics
Dan A. Simovici

Characterization of Partial She®er Functions in 3-valued Logic
Lucien Haddad, Dietlinde Lau

Power Indexes in Voting Systems and Multiple-Valued Logic
Yoshinori Yamamoto

Session 6B – Circuit Design 3 *(Chair: N. Homma)*
A Ternary Analog-to-Digital Converter System
Tomoki Tanoue, Munehiko Nagatani, Takao Waho

Configurable Multiple-Valued Encoders using Semi Floating-Gate Inverters
René Jensen, Yngvar Berg

Fault tolerant CMOS logic using ternary gates.
Yngvar Berg, Rene Jensen, Johannes Goplen Lomsdalen, Henning Gundersen, Snorre Aunet

11:05 - 11:10 Coffee Break

11:10 - 12:10 Session 7A and 7B

Session 7A – Theory 7 *(Chair: R .S. Stankovic)*
Universal VLSI Based on a Redundant Multiple-Valued Sequential Logic Operation
Tasuku Ito, Michitaka Kameyama

An Application of 16-Valued Logic to Design of Reconfigurable Logic Arrays
Tsutomu Sasao

LINEARIZATION OF TERNARY DECISION DIAGRAMS BY USING THE POLYNOMIAL CHRESTENSON SPECTRUM
Milena Stanković, Suzana Stojković, Claudio Moraga

Session 7B – Circuit Design 4 *(Chair: S. Aunet)*
Modeling a Fully Scalable Reed-Solomon Encoder/Decoder over GF(pm) in SystemC
Rolf Drechsler, André Sülflow

Design of a Processing Element Based on Quaternary Differential Logic for a Multi-Core SIMD Processor
Hirokatsu Shirahama, Akira Mochizuki, Takahiro Hanyu, Masami Nakajima, Kazutami Arimoto

Asynchronous Peer-to-Peer Simplex/Duplex-Compatible Communication System Using a One-Phase Signaling Scheme
Tomohiro Takahashi, Kazuyasu Mizusawa, Takahiro Hanyu

12:10 – 13:30 Lunch at Scandic Edderkoppen Hotel

May 15, Afternoon, Scandic Edderkoppen Hotel

13:30 – 14:50 Session 8A and 8B

Session 8A – Theory 8 *(Chair: C. Moraga)*
Classifications and basis enumerations in P3(2)
Dietlinde Lau, Masahiro Miyakawa

Simulation of Gate Circuits with Feedback in Multi-Valued Algebras
Janusz Brzozowski, Yuli Ye

Properties and Fast Algorithms for TernaryWalsh Transform
Bogdan J. Falkowski and Shixing Yan

Fuzzy Weighted and Ordered Direct Cover Algorithms for Minimization of MVL Functions
Mostafa Abd-El-Barr, Bambang A. B. Sarif

Session 8B – Circuit Design 5 *(Chair: R. Drechsler)*
Four-state Magnetic Random Access Memory and Ternary Content Addressable Memory using CoFe-based Magnetic Tunnel Junctions
Tetsuya Uemura, Takao Marukame, Ken-ichi Matsuda, Masafumi Yamamoto

Evaluation of Toggle Coverage for MVL Circuits Specified in the SystemVerilog HDL
Mahsan Amoui, Daniel Große, Mitchell A. Thornton, Rolf Drechsler

Limits to a Correct Evaluation in RTD-based Quaternary Inverters
Juan Núñez, José M. Quintana, María J. Avedillo

Evaluation and Comparison of Threshold Logic Gates
Lirigis Vasilios, Elena Dubrova

14:50 - 15:00 Coffee Break

15:00 – 16:00 Session 9A and 9B

Session 9A – Circuit Design 6 *(Chair: K. Berezowski)*
Towards First-Order Symbolic Trajectory Evaluation
Donglin Li, Otmane Ait-Mohamed, Sa'ed Abed

Survey of Stochastic Computation on Factor Graphs
Saeed Sharifi Tehrani, Shie Mannor, Warren J. Gross

A Note on Possible Applications of Fourier Representations in Circuit Design over Reprogrammable Technological Platforms
Radomir S. Stankovi´c, Jaakko Astola

Session 9B – Circuit Design 7 *(Chair: T. Waho)*
Quaternary Look-up Tables using voltage-mode CMOS Logic Design
Ricardo Cunha G. da Silva, Henri Boudinov

Active-Load Differential Comparator for Crosstalk-Noise Reduction
Akira Mochizuki, Masatomo Miura, Takahiro Hanyu

Experiment Result of Down Literal Circuit and Analog Inverter on CMOS Double-Polysilicon Process
Motoi Inaba

16:10 - 17:10 Plenary Session

18:30 – 19:30 A guided bus tour in the surroundings of Oslo.

Starting at Scandic Edderkoppen Hotel, and ends up at the Frogenerseteren Restaurant. A brief guided tour, showing the surroundings of Oslo. We will addend a small stop at the famous Holmekollen skijump arena, where it is possible to visit the tower of the ski jump for a beautiful view of Oslo on a clear day.

19:30 – 24:00 Banquet at Frognerseteren Restaurant

Frognerseteren offers dining facilities, café and restaurant in historical surroundings, high up in the Holmenkollen hills. The place has a magnificent view of the city and the Oslo Fjord, and a kitchen presenting the best of traditional Norwegian cooking.